a second pad arranged on a wiring layer different from the first I/O slot and comprising a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward the central portion;

a first wiring comprising one end positioned in said first pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

B1

a second wiring comprising one end positioned in the second pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

a third wiring arranged in an outermost peripheral portion of the chip and serving to connect the other end of the first wiring to the second I/O slot; and

a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot[, the fourth wiring being isolated from the first wiring].

9. (Amended) A semiconductor integrated circuit device, comprising

first and second I/O slots arranged on the same wiring layer in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip,

B2

a first pad arranged on a wiring layer different from the first I/O slot;

a second pad arranged on a wiring layer different from the first I/O slot and comprising a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward the central portion;

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

a first wiring comprising one end positioned in the first pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring comprising one end positioned in said second pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to the second I/O slot, and

a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, the fourth wiring being shorter than the third wiring.

B2 cont.

10. (Amended) The semiconductor integrated circuit device according to claim 9, wherein the third wiring is isolated from the second wiring, and the fourth wiring is isolated from the first wiring.

SUB C2

11. (Amended) The semiconductor integrated circuit device according to claim 9, wherein the third wiring and the fourth wiring do not overlap.

12. (Amended) The semiconductor integrated circuit device according to claim 9, wherein the first and second I/O slots, the first and second pads and the first and second wiring are each designed and fixed in advance.

13. (Amended) The semiconductor integrated circuit device according to claim 9, wherein the first wiring and the second wiring are the same in wiring level.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com